

# SPECIFICATION

Electronic Version 1.2.8

Stylesheet Version 1.0

---

## [HEXAGONAL GATE STRUCTURE FOR RADIATION RESISTANT FLASH MEMORY CELL]

### Background of Invention

[0001] Field of Invention

[0002] The present invention relates to a flash memory cell structure. More particularly, the present invention relates to a flash memory cell structure capable of resisting a high dose of radiation.

[0003] Description of Related Art

[0004] When a flash memory unit operates inside a radioactive environment, photons having energy in excess of 4.3eV may be transferred to electrons so that the electrons jump an energy barrier and radiate. If the electron is located within an oxide layer, the electron may be rapidly transferred to a substrate or control gate due to the effect of an electric field. In general, electrons lost in this manner may lead to a lowering of threshold voltage for the flash memory cells.

[0005] A conventional MNOS type of memory cell provides some radiation resistance. However, the coupling constant of a MNOS memory cell is too low to meet the demands of a flash memory.

[0006] In a conventional NROM memory cell structure, size of the drain terminal and the source terminal is almost identical, or else, the drain terminal is bigger than the source terminal. This often leads to source-side injection of the memory cell and problems such as second bit effect, thereby affecting the performance of the NROM.

[0007] Thus, although a MNOS memory cell is capable of resisting radiation, a low

coupling constant renders it useless as a flash memory cell. Yet, the popular NROM structure has some drawbacks including source-side injection and problems due to second bit effect. Thus, how to produce a radiation resistant NROM flash memory cell is still a major research topic.

## Summary of Invention

[0008] Accordingly, one object of the present invention is to provide a hexagonal gate flash memory cell capable of resisting intense radiation but having a reduced source-side injection as well as second bit effect so that the memory cell has a relatively constant threshold voltage despite operating in a radioactive environment.

[0009] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a radiation resistant hexagonal gate flash memory cell. The flash memory cell includes a substrate, a source region located within the substrate, a drain region also located within the substrate and a gate structure. The gate structure is formed over the substrate between the source region and the drain region. The gate structure further includes an oxide-nitride-oxide composite layer and a control gate layer sequentially stacked over the substrate. The gate structure has a hexagonal profile when viewed from the top. When the flash memory cell is subjected to radiation illumination, electron-hole pairs thus generated will be injected into the substrate without passing into the nitride layer.

[0010] This invention also provides a radiation resistant flash memory cell. The flash memory cell includes a substrate, a source region located within the substrate, a drain region also located within the substrate and a gate structure. A channel region is formed between the drain region and the source region. The gate structure is formed over the substrate between the source region and the drain region. The gate structure further includes an oxide-nitride-oxide composite layer and a control gate structure sequentially stacked over the substrate in a direction perpendicular to the channel region. Width of the gate structure increases from the source region to a pre-determined location. Thereafter, width of the gate structure decreases towards the drain region. When the flash memory cell is subjected to radiation illumination, electron-hole pairs thus generated will be injected into the substrate without passing

into the nitride layer.

[0011] This invention also provides an alternative radiation resistant flash memory cell. The flash memory cell includes a substrate, a source region, a drain region and a gate structure. A channel region is formed between the drain region and the source region. The gate structure is formed over the substrate between the source region and the drain region. The gate structure further includes an oxide-nitride-oxide composite layer. In a direction perpendicular to the channel region, width of the gate structure increases from the source region to a pre-determined location. Thereafter, width of the gate structure decreases towards the drain region. When the flash memory cell is subjected to radiation illumination, electron-hole pairs thus generated will be injected into the substrate without passing into the nitride layer. To program codes into the flash memory cell, the section of the gate structure close to the source region serves as an equivalent source region so that size of the equivalent source region is greater than the drain region, thereby preventing second bit effect.

[0012] In the aforementioned memory cell structure, the pre-determined location may lie close to the center of symmetry of the gate structure. In addition, width of the gate structure increases from the source region along a direction perpendicular to the channel up until the pre-determined location. Thereafter, width of the gate structure decreases towards the drain region. Such an expansion and contraction of width along a direction perpendicular to the channel ultimately forms a gate having a roughly hexagonal profile.

[0013] This invention also provides a radiation resistant flash memory cell. The flash memory cell includes a substrate, a source region, a drain region and a gate structure. A channel region is formed between the drain region and the source region. The gate structure is formed over the substrate between the source region and the drain region. The gate structure further includes an oxide-nitride-oxide composite layer. In a direction perpendicular to the channel region, width of the gate structure is greater than both the drain region and the source region. In other words, the gate structure has a wide waist profile. When the flash memory cell is subjected to radiation illumination, electron-hole pairs thus generated will be injected into the substrate without passing into the nitride layer. To program codes into the flash memory cell,

the section of the gate structure close to the source region serves as an equivalent source region so that size of the equivalent source region is greater than the drain region, thereby preventing second bit effect.

[0014] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

## Brief Description of Drawings

[0015] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0016] Fig. 1 is a schematic top view of a hexagonal gate flash memory cell fabricated according to this invention;

[0017] Fig. 2 is a cross-sectional view of a hexagonal gate flash memory cell fabricated according to this invention;

[0018] Fig. 3 is a cross-sectional view of a hexagonal gate flash memory cell fabricated according to this invention undergoing a programming operation; and

[0019] Fig. 4 is a schematic top view of a radiation resistant flash memory cell according to another embodiment of this invention.

## Detailed Description

[0020] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0021] According to the results of experiments and analysis, an oxide-nitride-oxide (ONO) structure and NROM type memory cell are both capable of resisting radiation illumination. However, the coupling constant of the ONO structure is much higher than the NROM memory cell. Hence, the ONO layer of the NROM memory cell, aside

from serving as an ideal trapping layer, may also serve as an excellent radiation protector.

[0022] Fig. 1 is a schematic top view of a hexagonal gate flash memory cell fabricated according to this invention. Fig. 2 is a cross-sectional view of a hexagonal gate flash memory cell fabricated according to this invention. The radiation resistant hexagonal gate flash memory cell 100 includes a substrate 130, a source region 112 located within the substrate 130, a drain region 110 also located within the substrate 130 and a gate structure 120. The gate structure 120 is above the substrate 130 between the source region 112 and the drain region 110. The gate structure 120 further includes an oxide layer 120a, a nitride layer 120b, an oxide layer 120c and a control gate layer 120d. The oxide layer 120a, the nitride layer 120b and the oxide layer 120c together form an oxide-nitride-oxide (ONO) composite layer. The ONO layer and the control gate layer 120d are sequentially stacked over the substrate 130. As shown in Fig. 2, a channel region 140 is formed in the substrate 130 between the source region 112 and the drain region 110.

[0023] One major aspect of this invention is in the gate structure 120 of the flash memory cell. As shown in Fig. 1, in a direction perpendicular to the channel 140, width W of the gate structure 120 increases gradually from the source region 112 to a pre-determined location. Thereafter, width of the gate structure 120 decreases gradually towards the drain region 110. Consequently, the gate structure 120 has a hexagonal profile when viewed from the top.

[0024] The energy barrier between the oxide layer 120a and the nitride layer 120b is far greater than the energy barrier between the oxide layer 120a and the substrate 130. Thus, the electron-hole pairs generated in the oxide layer 120 due to radiation are injected into the substrate 130 instead of the nitride layer 120b. Because the electron holes produced by radiation bypass the nitride layer 120b, trapped electrons inside the nitride layer 120b will not be neutralized. Hence, threshold voltage of the flash memory cell will remain at a constant value.

[0025] Fig. 3 is a cross-sectional view of a hexagonal gate flash memory cell fabricated according to this invention undergoing a programming operation. The hexagonal structure may be regarded as two separate trapezoidal gate structures that connect to

the source region 112 and the drain region 110 respectively. Thus, the hexagonal gate flash memory cell are equivalent to having two back to back gate structures 122 and 124 as shown in Fig. 1.

[0026] To program the flash memory cell, a portion of the gate structure 124 and the source region 112 can be regarded as an equivalent source region 112". Hence, size of the drain region is much smaller than the equivalent source region 112". During the programming operation, the equivalent channel length  $L_{eq}$  is also much shorter than the original channel length  $L$ . Therefore, hot electrons will exit the channel somewhere along the gate structure 120 to be subsequently trapped inside the nitride layer 120b after passing through the oxide layer 120a (Fig. 3).

[0027] Since the hot electrons inject into the nitride layer halfway through the channel (the side of equivalent source region 112") rather than from the original source region 112, trajectories of the hot electrons are little affected by the original electron distribution in the source region 112. In other words, source-side injection and second bit effect are prevented using a flash memory cell with this hexagonal gate structure.

[0028] Fig. 4 is a schematic top view of a radiation resistant flash memory cell according to another embodiment of this invention. As shown in Fig. 4, the flash memory includes a substrate, a source region 162, a drain region 160 and a gate structure 164. A channel is formed in the substrate between the drain region 160 and the source region 162. The gate structure 164 is formed over the substrate between the source region 162 and the drain region 160. The gate structure 164 has an oxide-nitride-oxide composite layer. In a direction perpendicular to the channel, width of the gate structure 164 is greater than both the source region and the drain region 160. In other words, the gate structure 164 has a wide waist.

[0029] When the flash memory cell is illuminated by radiation, electron-hole pairs will inject into the substrate instead of the nitride layer. Since holes produced by the radiation are diverted from the nitride layer 120b, electrons originally trapped inside the nitride layer 120b will not be neutralized. Ultimately, threshold voltage of the flash memory cell will remain constant. Furthermore, in a program coding operation, a portion of the gate structure 164 close to the source region 162 may serve as an

equivalent source region. Since the equivalent source region has a size much greater than the drain region, second bit effect is reduced considerably.

[0030] In summary, this invention utilizes the radiation resistant ONO layer inside a NROM memory cell together with a hexagonal or wide waist gate structure to prevent second bit effect and source-side injection.

[0031] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.